CLAIMS

1. A programmable memory cell formed in a p-type semiconductor substrate and useful in a memory array having column bitlines and row wordlines, the memory cell comprising:

a transistor having a p+ doped gate, a gate dielectric between the gate and over said substrate; and

wherein the second p+ doped semiconductor region of the transistor is connected to one of said row wordlines, and wherein said row wordline is formed by an n-type region near the surface of said semiconductor substrate.

2. The memory cell of Claim 1 wherein said gate is formed from one of said column bitlines.

3. The memory cell of Claim 1 wherein said memory cells further including a programmed doped region formed in said substrate in a channel region when said memory cell has been programmed.

4. A programmable memory cell formed in an n-type well and useful in a memory array having column bitlines and row wordlines, the memory cell comprising:

a transistor having a n+ doped gate, a gate dielectric between the gate and over a substrate; and

wherein the second n+ doped semiconductor region of the transistor is connected to one of said row wordlines, and wherein said row wordline is formed by a p-type region near the surface of said n-type well.

5. The memory cell of Claim 4 wherein said gate is formed from one of said column bitlines.

6. The memory cell of Claim 4 wherein said memory cells further including a programmed doped region formed in said substrate in a channel region when said memory cell has been programmed.

7. The memory cell of Claim 4 wherein said n-type well is replaced by an n-type substrate.

8. A programmable memory cell formed in a p-type semiconductor substrate and useful in a memory array comprising:

a plurality of column bitlines formed from p+ doped polysilicon, a dielectric between the plurality of column bitlines and over said substrate; and

a plurality of row wordlines formed by n-type regions near the surface of said semiconductor substrate and intersecting with said column bitlines but separated by said dielectric, wherein one of said memory cells is at the intersection of one of said column bitlines and one of said row wordlines.

9. The memory cell of Claim 8 wherein said memory cell further includes a programmed doped region formed in said substrate when said memory cell has been programmed.

10. The memory cell of Claim 8 wherein said dielectric is an oxide.

11. A programmable memory cell formed in an n-type well and useful in a memory array comprising:

a plurality of column bitlines formed from n+ doped polysilicon, a dielectric between the plurality of column bitlines and over a substrate; and

a plurality of row wordlines formed by p-type regions near the surface of said n-type well and intersecting with said column bitlines but separated by said dielectric, wherein one of said memory cells is at the intersection of one of said column bitlines and one of said row wordlines.

12. The memory cell of Claim 11 wherein said memory cell further includes a programmed doped region formed in said substrate when said memory cell has been programmed.

13. The memory cell of Claim 11 wherein said dielectric is an oxide.

14. The memory cell of Claim 8 wherein said n-type well is replaced by an n-type substrate.